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This index covers all technical items - papers, correspondence, reviews, etc. - that appeared in this periodical during 1995, and items from previous years that were commented upon or corrected in 1995.

The Author Index contains the primary entry for each item, listed under the first author's name, and cross-references from all coauthors. The Subject Index contains several entries for each item under appropriate subject headings, and subject cross-references.

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 FPAD, fuzzy nonlin. prog. approach, analog cct. design. *Fares, M.*, +, *T-CAD Jul 95* 785-793
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Architecture, computer; cf. Computer architecture
Arrays; cf. Logic arrays
Artificial intelligence; cf. Inference mechanisms; Knowledge based systems
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Automation; cf. Automatic testing; Design automation

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BiCMOS digital integrated circuits

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Binary sequences

BIST for VLSI ccts., test embedding, discrete logarithms. *Lempel, M.*, *T-CAD May 95* 554-566

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Bipolar analog integrated circuits

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Bipolar digital integrated circuits

VLSI bipolar cct. simul. techs. based on waveform relax. *Wen Fang*, *T-CAD Apr 95* 510-518

Bipolar digital integrated circuits; cf.

 BiCMOS digital integrated circuits
 Emitter coupled logic

Bipolar transistors

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Bipolar transistors; cf.

 Heterojunction bipolar transistors

BIST (built-in self-test); cf.

 Self-testing

Boolean functions

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Boolean functions; cf.

 Logic functions

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Boundary value problems

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Built-in testing; cf.

 Self-testing

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CAD (computer aided design); cf.

 Design automation software; Design automation

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Carrier processes; cf.

 Charge carrier processes

CASE; cf.

 Computer aided software engineering

Cellular automata

2D cellular automata for parallel logic and fault simul. *Yih-Lang Li*, *T-CAD Jun 95* 740-749

Cellular logic arrays

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std. cells, pin permutation algm. for improving over-the-cell channel routing. *Chen, C.Y.R.*, +, *T-CAD Aug 95* 1030-1037

- VLSI layout CAD, optimal net assignment, constraints. *Ting-Chi Wang*, +, *T-CAD Feb 95* 265-269
- Charge carrier processes**
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- Circuit analysis; cf.** Circuit transient analysis
Circuit boards; cf. Layout of circuit boards
Circuit design; cf. Circuit synthesis; Logic design
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 VLSI, optimal wiresizing under Elmore delay model. *Gong, J.J.*, +, *T-CAD Mar 95* 321-336
 VLSI timing optim. by gate resizing and crit. path ident. *Chen-Liang Fang*, +, *T-CAD Feb 95* 201-217
- Circuit optimization; cf.** Layout of circuit boards
Circuit reliability; cf. Integrated circuit reliability
Circuits; cf. Adders; Distributed parameter circuits; Equivalent circuits; Feedback circuits; Integrated circuit...; Interconnected circuits; Large-scale circuits; Linear circuits; Lossy circuits; Multiport circuits; Non-linear circuits; Switching circuits
- Circuit simulation**
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- Circuit stability**
 SPICE dc operating point anal., identifying unstable operating points, IC design. *Green, M.M.*, +, *T-CAD Mar 95* 360-370
- Circuit stability; cf.** Oscillator stability
- Circuit synthesis**
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- Circuit testing; cf.** Integrated circuit testing
- Circuit topology**
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- Circuit transient analysis**
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- Clocks**
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 VLSI digital ccts., power/ground buses, pattern independent max. current estim. *Kriplani, H.*, +, *T-CAD Aug 95* 998-1012

CMOS digital integrated circuits; cf. BiCMOS digital integrated circuits**CMOSFET logic devices**

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CMOS integrated circuits

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CMOS integrated circuits; cf. CMOS analog integrated circuits; CMOS digital integrated circuits; CMOSFETs**Coding/decoding; cf. Encoding****Cognitive science; cf. Inference mechanisms****Combinational logic circuit fault diagnosis**

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Combinational logic circuit fault diagnosis; cf. Combinational logic circuit testing**Combinational logic circuits**

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 efficient exhaustive test set generation. *Stanion, R.T.*, +, *T-CAD Dec 95* 1516-1525

NEST nonenumerative test generation method. path delay fault. *Pomeranz, I.*, +, *T-CAD Dec 95* 1505-1515
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Combinatorial mathematics; cf. Graph theory**Complementary MOS; cf. CMOSFETs; CMOS integrated circuits****Complexity theory**

area-time optimal testable adders, generation method. *Becker, B.*, *T-CAD Sep 95* 1049-1066
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SIERA, unified framework for prototyping of syst.-level hardware/software. *Srivastava, M.*, +, *T-CAD Jun 95* 676-693

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Computer interfaces; cf. User interfaces**Computer languages; cf. Hardware design languages****Computer pipeline processing; cf. Pipeline processing****Computer programming; cf. Computer aided software engineering; Software design/development****Computer reliability; cf. Computer fault tolerance****Computers; cf. Parallel processing****Concurrent engineering**

SIERA, unified framework for prototyping of syst.-level hardware/software. *Srivastava, M.*, +, *T-CAD Jun 95* 676-693

Control systems; cf. Observability**Convergence of numerical methods**

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MCM lossy coupled transm. line trees, time domain response, efficient approx. *Sriram, M.*, +, *T-CAD Aug 95* 1013-1024
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Current measurement

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- VLSI, optimal wiring sizing under Elmore delay model. *Gong, J.J.*, +, *T-CAD Mar 95* 321-336
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- Design automation software**
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- Design methodology; cf. Design automation**
- Detectors**
- built-in current sens. for static CMOS realizations. *Jien-Chung Lo*, *T-CAD Nov 95* 1402-1407
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- Dielectric films**
- BPSG insulating film thermal flow, 3D modeling, surface diffusion. *Fujinaga, M.*, +, *T-CAD May 95* 631-638
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- Diffusion processes**
- BPSG insulating film thermal flow, 3D modeling, surface diffusion. *Fujinaga, M.*, +, *T-CAD May 95* 631-638
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- Digital integrated circuits**
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- Digital system fault diagnosis**
- act. timing multilevel fault-simul., switch-level accuracy. *Meyer, W.*, *T-CAD Oct 95* 1241-1256
- Digital systems**
- max.-rate single-phase closed pipeline clocking including wave pipelining/stoppability/startability. *Chang, C.-H.*, +, *T-CAD Dec 95* 1526-1545
- Diodes; cf. Semiconductor diodes**
- Directed graphs**
- 2D cellular automata for parallel logic and fault simul. *Yih-Lang Li*, *T-CAD Jun 95* 740-749
- Directed graphs; cf. Petri nets**
- Discrete time filters; cf. Switched capacitor filters**
- Dissipative circuits; cf. Lossy circuits**
- Dissipative systems; cf. Lossy systems**
- Distortion; cf. Delay effects**
- Distributed parameter circuits**
- CFH, complex freq. hopping anal. of interconnect networks. *Chiprout, J.*, +, *T-CAD Feb 95* 186-200
- Dynamic programming**
- area-time optimal testable adders, generation method. *Becker, B.*, *T-CAD Sep 95* 1049-1066
- stacked layouts in CMOS analog ccts., automatic generation algm. *Malavasi, E.*, +, *T-CAD Jan 95* 107-122
- VLSI multiway partitioning via geometric embeddings, orderings, and dyn. prog. *Alpert, C.J.*, +, *T-CAD Nov 95* 1342-1358

E

ECL; cf. Emitter coupled logic

Eigenvalues/eigenfunctions

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Eigenvalues/eigenfunctions; cf. Poles and zeros
Electric variables; cf. Capacitance
Electric variables measurement; cf. Current measurement
Electromagnetic analysis
 photolithography, massively parallel EM simul. *Wong, A.K.*, +, *T-CAD Oct 95 1231-1240*
Electromagnetic interference; cf. Crosstalk
Electromagnetic transient analysis; cf. Switching transients
Emitter coupled logic
 functional verification algm. *Brauer, E.J.*, +, *T-CAD Dec 95 1546-1556*
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 IC proc. simul., grid adaption. *Law, M.E.*, *T-CAD Oct 95 1223-1230*

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Fabrication; cf. Integrated circuit fabrication
Fault diagnosis
 current-mode ADCs, test gen. and concurrent error detect. *Chin-Long Wey*, +, *T-CAD Oct 95 1291-1298*
 uneven fault coverage in ICs, quality reduction. *Maxwell, P.C.*, *T-CAD May 95 603-607*
Fault diagnosis; cf. Digital system fault diagnosis; Logic circuit fault diagnosis
Fault tolerance
 non-tree routing topologies for VLSI layout. *McCoy, B.A.*, +, *T-CAD Jun 95 780-784*
Fault tolerance; cf. Computer fault tolerance
FDTD methods
 photolithography, massively parallel EM simul. *Wong, A.K.*, +, *T-CAD Oct 95 1231-1240*
Feedback amplifiers; cf. Operational amplifiers
Feedback circuits
 CMOS ccts., current testability anal. of feedback bridging faults. *Roca, M.*, +, *T-CAD Oct 95 1299-1305*
FET analog integrated circuits; cf. MOS analog integrated circuits
FET digital integrated circuits; cf. MOS digital integrated circuits
FET integrated circuits; cf. MOS integrated circuits
FET logic devices; cf. MESFET logic devices
FETs; cf. MESFETs
Films; cf. Dielectric films
Filters; cf. FIR digital filters; IIR digital filters; Switched capacitor filters
Finite automata; cf. Cellular automata; Finite state machines
Finite difference methods
 interconnect capacit. of ICs, automatic model generation. *Choudhury, U.*, +, *T-CAD Apr 95 470-480*
 TRASIM, 2D transient simulator for planar semicond. devices. *Obrecht, M.S.*, +, *T-CAD Apr 95 447-458*
 VLSI RC parasitics modeling based on network reduction algm. *Niewczas, M.*, +, *T-CAD Feb 95 137-144*
Finite difference time domain methods; cf. FDTD methods
Finite duration impulse response digital filters; cf. FIR digital filters
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 hydrodyn. semicond. eqns., Taylor-Galerkin FEA. *Bova, S.*, +, *T-CAD Dec 95 1437-1444*
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Flow graphs; cf. Data flow graphs; Signal flow graphs
Frequency domain analysis
 CFH, complex freq. hopping anal. of interconnect networks. *Chiprout, E.*, +, *T-CAD Feb 95 186-200*
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 combinat. logic cct. delay, functional timing anal., ATPG. *Ashar, P.*, +, *T-CAD Aug 95 1025-1030*
Functions; cf. Boolean functions; Transfer functions
Fuzzy sets
 FPAID, fuzzy nonlin. prog. approach, analog cct. design. *Fares, M.*, +, *T-CAD Jul 95 785-793*

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Galerkin's method; cf. Moment methods
Gallium materials/devices
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Genetic algorithms
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Germanium materials/devices
 heterojunction devices, FEA. *Krishna, G.H.R.*, +, *T-CAD Jul 95 803-814*
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 PLA minimization, graph-based output phase assignment. *Yanbing Xu*, +, *T-CAD May 95 613-622*
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 VLSI multiway partitioning via geometric embeddings, orderings, and dyn. prog. *Alpert, C.J.*, +, *T-CAD Nov 95 1342-1358*

Graph theory; cf. Data flow graphs; Directed graphs; Signal flow graphs; Trees (graphs)

H

Hardware design languages

- IC layouts comparison with HDL models, formal verif. tech. *Kam, T.*, + , *T-CAD Apr 95* 503-509
SpecCharts, VHDL front-end for embedded sys. *Vahid, F.*, + , *T-CAD Jun 95* 694-706

Harmonic distortion

- Nyquist data converters, verif., behavioral simul. *Liu, E.*, + , *T-CAD Apr 95* 493-502

HDL; cf.

 Hardware design languages

Heterojunction bipolar transistors

- SiGe heterojunction devices, finite element anal. *Krishna, G.H.R.*, + , *T-CAD Jul 95* 803-814

High-speed integrated circuits

- CMOS VLSI digital ccts., delay optim., transistor reordering. *Carlson, B.S.*, + , *T-CAD Oct 95* 1183-1192

I

Identification

- path delay fault testability synthesis, tautology-based untestability ident./factorization. *Fuchs, K.*, *T-CAD Dec 95* 1470-1479

IGFETs; cf.

 MOSFETs

IIR digital filters

- symbolic anal. of SC filtering networks, sig. flow graphs. *Fino, M.H.*, + , *T-CAD Jul 95* 858-867

Inductive transducers; cf.

 Magnetic transducers

Inference mechanisms

- MOS analog IC design automation, automated cct. correction, qualitat. reasoning. *Makris, C.A.*, + , *T-CAD Feb 95* 239-254
symbolic trajectory eval. and BDDs, theorem prover, VLSI design. *Hazelhurst, S.*, + , *T-CAD Apr 95* 413-422

Infinite duration impulse response digital filters; cf.

 IIR digital filters

Information theory; cf.

 Encoding

Integer programming

- cell-level analog ccts., integer prog. based topol. selection. *Maulik, P.C.*, + , *T-CAD Apr 95* 401-412
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Integral equations; cf.

 Moment methods

Integrated circuit design

- behavioral level testability, partial scan cost minimization. *Potkonjak, M.*, + , *T-CAD May 95* 531-546
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VLSI voltage depend. capacitance model, mfg. proc. effects on voltage coeffs. *Ito, A.*, *T-CAD Sep 95* 1093-1097
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Integrated circuit design; cf.

 Hardware design languages; Layout of integrated circuits

Integrated circuit fabrication

- uneven fault coverage in ICs, quality reduction. *Maxwell, P.C.*, *T-CAD May 95* 603-607

Integrated circuit fabrication; cf.

 Lithography

Integrated circuit interconnections

- automatic model generation for interconnect capacit. *Choudhury, U.*, *T-CAD Apr 95* 470-480
CFH, complex freq. hopping anal. of interconnect networks. *Chiprout, J.*, + , *T-CAD Feb 95* 186-200
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VLSI, optimal wiring under Elmore delay model. *Gong, J.J.*, *T-CAD Mar 95* 321-336

Integrated circuit manufacture; cf.

 Integrated circuit fabrication

Integrated circuit metallization; cf.

 Integrated circuit interconnections

Integrated circuit modeling

- CMOS mixed sig. ccts., substr. coupling models based on Voronoi tessellation. *Wemple, I.L.*, + , *T-CAD Dec 95* 1459-1469
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HDL models comparison with layouts, formal verif. tech. *Kam, T.*, *T-CAD Apr 95* 503-509
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VLSI RC parasitics modeling based on network reduction algm. *Niewicz, M.*, + , *T-CAD Feb 95* 137-144
VLSI voltage depend. capacitance model, mfg. proc. effects on voltage coeffs. *Ito, A.*, *T-CAD Sep 95* 1093-1097

Integrated circuit noise

- Nyquist data converters, verif., behavioral simul. *Liu, E.*, + , *T-CAD Apr 95* 493-502
VLSI cct. performs., worst-case anal. and optim. *Dharchoudhury, A.*, *T-CAD Apr 95* 481-492

Integrated circuit packaging; cf.

 Multichip modules

Integrated circuit reliability

- CMOS VLSI digital ccts., power/ground buses, pattern independent moment estim. *Kriplani, H.*, + , *T-CAD Aug 95* 998-1012
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Integrated circuits; cf.

 Analog integrated circuits; Application specific integrated circuits; Digital integrated circuits; High-speed integrated circuits; Large-scale integration; Monolithic integrated circuits

Integrated circuit testing

- 12th IEEE VLSI Test Symposium, selected papers (special issue). *T-CAD May 95* 529-612
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BIST lin. compactors, fast signature comp. algm. *Lambidonis, D.*, *T-CAD Aug 95* 1037-1044
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- cct.-level dictionaries of CMOS bridging faults. *Lee, T.*, +, *T-CAD May 95* 596-603
- CMOS ccts., current testability anal. of feedback bridging faults. *Roca, M.*, +, *T-CAD Oct 95* 1299-1305
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- pseudo-exhaustive testing, VLSI ccts., cct. partitioning and test generation method. *Wen-Ben Jone*, +, *T-CAD Mar 95* 374-384
- seq. ccts., test efficiency anal. of random self-test. *Pilarski, S.*, *T-CAD Aug 95* 1044-1045
- seq. ccts. with scan, full or partial, test appl. time reduction. *Soo Young Lee*, +, *T-CAD Sep 95* 1128-1140
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- uneven fault coverage in ICs, quality reduction. *Maxwell, P.C.*, *T-CAD May 95* 603-607
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- large ccts., testable design, partition and resynthesis. *Kanjilal, S.*, +, *T-CAD Oct 95* 1268-1276
- seq. cct. test fn. embedding algms., interconnected finite state machines. *Kanjilal, S.*, +, *T-CAD Sep 95* 1115-1127
- interconnected circuits; cf.** Large-scale circuits
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- interpolation; cf.** Digital-analog conversion
- iterative logic arrays; cf.** Cellular logic arrays
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- 3D MOSFET simul., massively parallel computation, splitting-up operator. *Odanaka, S.*, +, *T-CAD Jul 95* 824-832
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- submicron devices, modeling and simul., transport effects and charact. modes. *Jerome, J.W.*, +, *T-CAD Aug 95* 917-923

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Large-scale circuits; cf. Interconnected circuits

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- submicron LSI layout, perform. driven spacing algms. *Onozawa, A.*, +, *T-CAD Jun 95* 707-719

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- Logic circuit design; cf. Logic design**
- Logic circuit fault diagnosis**
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- Logic circuit fault diagnosis; cf. Combinational logic circuit fault diagnosis**
- Logic circuit testing; cf. Asynchronous logic circuits; Combinational logic circuits; Logic arrays; Logic modules; MOS digital integrated circuits; Multivalued logic circuits; Sequential logic circuits**
- Logic circuit testing**
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- Logic design**
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- Logic functions; cf. Boolean functions**
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Mathematical programming; cf. Dynamic programming; Linear programming; Nonlinear programming
Mathematics; cf. Functional analysis; Numerical analysis; Optimization methods
Matrices; cf. Jacobian matrices; Moment methods; Sparse matrices
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MESFET logic devices
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 VLSI voltage depend. capacitance model, mfg. proc. effects on voltage coeffs. *Ito, A.*, *T-CAD Sep 95* 1093-1097
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Monolithic integrated circuits
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MOS digital integrated circuits
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Multichip modules
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Multivalued logic
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Negative resistance devices; cf. Tunnel diodes
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Nonlinear oscillators
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Numerical analysis

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Numerical analysis; cf. Convergence of numerical methods; Finite difference methods; Finite element methods; Iterative methods; Moment methods; Monte Carlo methods; Newton's method; Relaxation methods; Sparse matrices

Numerical stability

lin. cct. anal. by Pade approx. via Lanczos proc. *Feldmann, P.*, +, *T-CAD May 95* 639-649

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Observability

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Operational amplifiers

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Optimization methods

generalized optimum path search. *Tetelbaum, A.Y.*, *T-CAD Dec 95* 1586-1590

Optimization methods; cf. Circuit optimization; Genetic algorithms; Gradient methods; Mathematical programming; Minimization methods; Simulated annealing

Oscillators; cf. Nonlinear oscillators; Relaxation oscillators

Oscillator stability

nonlin. oscillatory ccts., steady-state output determ., multiple shooting. *Parkhurst, J.R.*, +, *T-CAD Jul 95* 882-889

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Parallel processing

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photolithography, massively parallel EM simul. *Wong, A.K.*, +, *T-CAD Oct 95* 1231-1240

Parallel processing; cf. Pipeline processing

Parallel programming; cf. Parallel algorithms

Partial differential equations; cf. Laplace equations

Perturbation methods

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Petri nets

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Phase distortion; cf. Delay effects

Photolithography

massively parallel EM simul. program. *Wong, A.K.*, +, *T-CAD Oct 95* 1231-1240

Pipeline processing

2D cellular automata for parallel logic and fault simul. *Yih-Lang Li*, +, *T-CAD Jun 95* 740-749

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PLA; cf. Programmable logic arrays

Placement; cf. Layout of integrated circuits

Poles and zeros

lin. cct. anal. by Pade approx. via Lanczos proc. *Feldmann, P.*, +, *T-CAD May 95* 639-649

Polynomials

BIST for VLSI ccts., test embedding, discrete logarithms. *Lempel, M.*, +, *T-CAD May 95* 554-566

Printed circuits; cf. Layout of circuit boards

Probabilistic differential equations; cf. Stochastic differential equations

Probability

BIST for VLSI ccts., test embedding, discrete logarithms. *Lempel, M.*, *T-CAD May 95* 554-566

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Nyquist data converters, verif., behavioral simul. *Liu, E.*, +, *T-CAD 95* 493-502

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Probability; cf. Monte Carlo methods

Programmable logic arrays

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minimization, output phase assignment, graph-based approach. *Yanbo Xu*, +, *T-CAD May 95* 613-622

Programming; cf. Computer aided software engineering; Software sign/development

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Quality control

uneven fault coverage in ICs, quality reduction. *Maxwell, P.C.*, *T-CAD May 95* 603-607

Quantization; cf. Analog-digital conversion

Quantum effect semiconductor devices; cf. Quantum well devices

Quantum well devices

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Real time systems

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SpecCharts, VHDL front-end for embedded sysys. *Vahid, F.*, +, *T-CAD Jun 95* 694-706

Reasoning; cf. Inference mechanisms

Redundancy

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multilevel logic optim. by redundancy addit. and removal. *Entrena, L.*, +, *T-CAD Jul 95* 909-916

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Registers; cf. Shift registers

Relaxation methods

MOSFET ccts., relax.-based transient sensitivity computation. *Chen-Jung Chen*, +, *T-CAD Feb 95* 173-185

Relaxation methods; cf. Simulated annealing

Relaxation oscillators

nonlin. oscillatory ccts., steady-state output determ., multiple shooting. *Parkhurst, J.R.*, +, *T-CAD Jul 95* 882-889

Relaxation oscillators; cf. Flip-flops

Reliability; cf. Fault tolerance; Quality control

Resonant tunneling devices

device and cct. simul. of quantum electronic devices. *Mohan, S.*, *T-CAD Jun 95* 653-662

hysteretic I-V charact. modeling for reson. tunneling diodes. *Ming-Hong Shieh*, +, *T-CAD Sep 95* 1098-1103

large-sig. DC model, PSPICE, three-state memory cct. *Zhixin Yan*, *T-CAD Feb 95* 167-172

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Roots; cf. Poles and zeros

Rough surfaces

BPSG insulating film thermal flow, 3D modeling, surface diffusion. *Fujinaga, M.*, +, *T-CAD May 95* 631-638

Routing; cf. Layout of integrated circuits

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Scheduling

- appl. specific instruction sets, synthesis. *Ing-Jer Huang*, +, *T-CAD Jun 95* 663-675
- area-efficient testable designs, behavioral synthesis, hardware sharing and partial scan. *Potkonjak, M.*, +, *T-CAD Sep 95* 1141-1154
- datapath synthesis, problem-space genetic algm. *Dhodhi, M.K.*, +, *T-CAD Aug 95* 934-944
- force-directed scheduling in high-throughput DSP systs. *Verhaegh, W.F.J.*, +, *T-CAD Aug 95* 945-960

Schottky FETs; cf. MESFETs

Search methods

- generalized optimum path search. *Tetelbaum, A.Y.*, *T-CAD Dec 95* 1586-1590
- HYPER-LP, high-level synthesis syst., appl. specific datapath intensive CMOS ccts. *Chandrakasan, A.P.*, +, *T-CAD Jan 95* 12-31
- stack of equal width components, folding tech. for chip archits. *Thanvantri, V.*, +, *T-CAD Jun 95* 775-780

Search methods; cf. Genetic algorithms

Self-testing

- controllable self-checking checkers for conditional concurrent checking. *Tarnick, S.*, *T-CAD May 95* 547-553
- C-testable iter. logic arrays, BIST. *Gala, M.*, +, *T-CAD Nov 95* 1388-1398
- current sens., built-in type for static CMOS realizations. *Jien-Chung Lo*, +, *T-CAD Nov 95* 1402-1407
- fast signature computation for BIST lin. compactors. *Lambidonis, D.*, +, *T-CAD Aug 95* 1037-1044
- multiple-input signature registers in BIST designs, shrinkage. *Savir, J.*, *T-CAD Nov 95* 1379-1387
- pseudo-exhaustive built-in TPG for seq. ccts. *Kagaris, D.*, +, *T-CAD Sep 95* 1160-1171
- pseudo-exhaustive testing, VLSI ccts., cct. partitioning and test generation method. *Wen-Ben Jone*, +, *T-CAD Mar 95* 374-384
- seq. ccts., test efficiency anal. of random self-test. *Pilarski, S.*, *T-CAD Aug 95* 1044-1045
- VLSI ccts., test embedding, discrete logarithms. *Lempel, M.*, +, *T-CAD May 95* 554-566

Semiconductor device fabrication; cf. Integrated circuit fabrication; Lithography

Semiconductor device modeling

- 3D MOSFET simul., massively parallel computation, splitting-up operator. *Odanaka, S.*, +, *T-CAD Jul 95* 824-832
- C_{∞} -continuous small-sig. model for MOS transistor in normal operation, IC simul. *Iniguez, B.*, +, *T-CAD Feb 95* 163-166
- explicit method for resolu. of semicond. device eqns. *Pleumeekers, J.L.*, +, *T-CAD Apr 95* 459-463
- hydrodyn. semicond. eqns., Taylor-Galerkin FEA. *Bova, S.*, +, *T-CAD Dec 95* 1437-1444
- hysteretic I-V charact. modeling for reson. tunneling diodes. *Ming-Huei Shieh*, +, *T-CAD Sep 95* 1098-1103
- magnetotransistors, mag. field sensit. modelling, HSPICE. *Salim, A.*, +, *T-CAD Apr 95* 464-469
- MOSFET device simul., optimum artificial diffusivity, flux dens. discretization. *Ting-Wei Tang*, +, *T-CAD Nov 95* 1309-1315
- quantum electronic devices, device and cct. simul. *Mohan, S.*, +, *T-CAD Jun 95* 653-662
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- Si devices, thermal noise in math. models of quasi-homogen. regions. *Mamontov, Y.V.*, +, *T-CAD Jul 95* 815-823
- SiGe heterojunction devices, finite element anal. *Krishna, G.H.R.*, +, *T-CAD Jul 95* 803-814
- submicron DC MOSFET model, analog cct. simul. *Chatterjee, A.*, +, *T-CAD Oct 95* 1193-1207
- submicron devices, modeling and simul., transport effects and charact. modes. *Jerome, J.W.*, +, *T-CAD Aug 95* 917-923
- template-based MOSFET device model. *Graham, M.G.*, +, *T-CAD Aug 95* 924-933
- TRASIM, 2D transient simulator for planar semicond. devices. *Obrecht, M.S.*, +, *T-CAD Apr 95* 447-458

Semiconductor device modeling; cf. Integrated circuit modeling

Semiconductor device noise

- Si devices, thermal noise in math. models of quasi-homogen. regions. *Mamontov, Y.V.*, +, *T-CAD Jul 95* 815-823

Semiconductor device noise; cf. Integrated circuit noise

Semiconductor device reliability; cf. Integrated circuit reliability

Semiconductor devices; cf. Semiconductor diodes

Semiconductor device testing; cf. Integrated circuit testing

Semiconductor device thermal factors

- SiGe heterojunction devices, finite element anal. *Krishna, G.H.R.*, +, *T-CAD Jul 95* 803-814

Semiconductor diodes

- SiGe heterojunction devices, finite element anal. *Krishna, G.H.R.*, +, *T-CAD Jul 95* 803-814
- submicron devices, modeling and simul., transport effects and charact. modes. *Jerome, J.W.*, +, *T-CAD Aug 95* 917-923

Semiconductor diodes; cf. Tunnel diodes

Semiconductor diode switches

- hysteretic I-V charact. modeling for reson. tunneling diodes. *Ming-Huei Shieh*, +, *T-CAD Sep 95* 1098-1103

Semiconductor materials

- SiGe heterojunction devices, finite element anal. *Krishna, G.H.R.*, +, *T-CAD Jul 95* 803-814

Semiconductor memory circuits

- RTD large-sig. DC model suitable for PSPICE. *Zhixin Yan*, +, *T-CAD Feb 95* 167-172

Semiconductor noise; cf. Semiconductor device noise

Semiconductor process modeling

- BPSG insulating film thermal flow, 3D modeling, surface diffusion. *Fujinaga, M.*, +, *T-CAD May 95* 631-638
- cellular based topography simul., algms. and models. *Strasser, E.*, +, *T-CAD Sep 95* 1104-1114
- IC proc. simul., grid adaption. *Law, M.E.*, *T-CAD Oct 95* 1223-1230
- photolithography, massively parallel EM simul. *Wong, A.K.*, +, *T-CAD Oct 95* 1231-1240
- TCAD syst., VISTA user interface and task level. *Halama, S.*, +, *T-CAD Oct 95* 1208-1222

Semiconductor switches; cf. Semiconductor diode switches

Sensitivity

- magnetotransistors, mag. field sensit. modelling, HSPICE. *Salim, A.*, +, *T-CAD Apr 95* 464-469
- MOSFET ccts., relax.-based transient sensitivity computations. *Chen-Jung Chen*, +, *T-CAD Feb 95* 173-185

Sensors; cf. Detectors

Sequences; cf. Binary sequences

Sequential logic circuit fault diagnosis

- 2D cellular automata for parallel logic and fault simul. *Yih-Lang Li*, +, *T-CAD Jun 95* 740-749
- full/partial scan, test appl. time reduction, seq. ccts. *Soo Young Lee*, +, *T-CAD Sep 95* 1128-1140
- multicycle false paths in perform. optim. of seq. logic ccts. *Ashar, P.*, +, *T-CAD Sep 95* 1067-1075
- untestable fault ident. in seq. ccts., combinat. ATPG theorems. *Agrawal, V.D.*, +, *T-CAD Sep 95* 1155-1160

Sequential logic circuit fault diagnosis; cf. Sequential logic circuit testing

Sequential logic circuits

- IC layouts comparison with HDL models, formal verif. tech. *Kam, T.*, +, *T-CAD Apr 95* 503-509
- multilevel logic optim. by redundancy addit. and removal. *Entrena, L.A.*, +, *T-CAD Jul 95* 909-916
- std.-cell VLSI cct. design, timing/area optim. *Weitong Chuang*, +, *T-CAD Mar 95* 308-320
- VLSI bipolar cct. simul. techs. based on waveform relax. *Wen Fang*, +, *T-CAD Apr 95* 510-518

Sequential logic circuit testing

- area-efficient testable designs, behavioral synthesis, hardware sharing and partial scan. *Potkonjak, M.*, +, *T-CAD Sep 95* 1141-1154
- fn. embedding algms., interconnected finite state machines. *Kanjilal, S.*, +, *T-CAD Sep 95* 1115-1127
- large ccts., testable design, partition and resynthesis. *Kanjilal, S.*, +, *T-CAD Oct 95* 1268-1276
- path-delay-fault testable nonscan seq. ccts. *Wuudiann Ke*, +, *T-CAD May 95* 576-582
- pseudo-exhaustive built-in TPG for seq. ccts. *Kagaris, D.*, +, *T-CAD Sep 95* 1160-1171
- random self-test, test efficiency anal. *Pilarski, S.*, *T-CAD Aug 95* 1044-1045
- reducing test appl. time, full scan ccts. *Pradhan, D.K.*, +, *T-CAD Dec 95* 1577-1586
- synthesis for testability techs. *Keutzer, K.*, +, *T-CAD Dec 95* 1569-1577

Set theory; cf. Fuzzy sets

Shift registers

- BIST for VLSI ccts., test embedding, discrete logarithms. *Lempel, M.*, +, *T-CAD May 95* 554-566
- pseudo-exhaustive testing, VLSI ccts., cct. partitioning and test generation method. *Wen-Ben Jone*, +, *T-CAD Mar 95* 374-384

Signal analysis; cf. Spectral analysis

Signal flow graphs

- asynchronous cct. synthesis, Boolean satisfiability. *Jun Gu, +, T-CAD Aug 95 961-973*
- clustering of ccts., stochastic flow injection method. *Ching-Wei Yeh, +, T-CAD Feb 95 154-162*
- CMOS transistor sig. flow direction assignment, integrated syst. *Lee, K.-J., +, T-CAD Dec 95 1445-1458*
- symbolic anal. of SC filtering networks, sig. flow graphs. *Fino, M.H., +, T-CAD Jul 95 858-867*
- two-way partitioning, optim. by iter. improvement, expt. eval. *Ching-Wei Yeh, +, T-CAD Feb 95 145-153*

Signal processing

- quadratic zero-one prog.-based synthesis of appl.-specific data paths. *Geurts, W., +, T-CAD Jan 95 1-11*

Signal processing; cf. Encoding; Estimation

Signal sampling/reconstruction; cf. Analog-digital conversion; Digital-analog conversion

Silicon materials/devices

- Si devices, thermal noise in math. models of quasi-homogen. regions. *Mamontov, Y.V., +, T-CAD Jul 95 815-823*

Simulated annealing

- appl. specific instruction sets, synthesis. *Ing-Jer Huang, +, T-CAD Jun 95 663-675*
- ASIC row-based cell placement method utilizing cct. structural props. *Yu-Wen Tsay, +, T-CAD Mar 95 393-397*
- row-based placement, simulated annealing, hierarchical algm., MCNC benchmark ccts. *Wern-Jieh Sun, +, T-CAD Mar 95 349-359*
- two-way partitioning, optim. by iter. improvement, expt. eval. *Ching-Wei Yeh, +, T-CAD Feb 95 145-153*

Simulation

- explicit method for resoln. of semicond. device eqns. *Pleumeekers, J.L., +, T-CAD Apr 95 459-463*
- interconnect capacit. of ICs, automatic model generation. *Choudhury, U., +, T-CAD Apr 95 470-480*
- magnetotransistors, mag. field sensit. modelling, HSPICE. *Salim, A., +, T-CAD Apr 95 464-469*
- TRASIM, 2D transient simulator for planar semicond. devices. *Obrecht, M.S., +, T-CAD Apr 95 447-458*

Simulation; cf. Circuit simulation

Software; cf. Automatic test software; Design automation software

Software design/development

- SIERA, unified framework for prototyping of syst.-level hardware/software. *Srivastava, M., +, T-CAD Jun 95 676-693*

Software engineering; cf. Computer aided software engineering; Software design/development

Sparse matrices

- 3D MOSFET simul., massively parallel computation, splitting-up operator. *Odanaka, S., +, T-CAD Jul 95 824-832*
- levelized incomplete LU factorization, large-scale cct. simul. appl. *Eickhoff, K.-M., +, T-CAD Jun 95 720-727*

Special issues/sections

- 12th IEEE VLSI Test Symposium, selected papers (special issue). *T-CAD May 95 529-612*

Spectral analysis

- logic cct. design, spectral coeffs. *Thornton, M.A., +, T-CAD Nov 95 1328-1341*

SPICE

- C_∞-continuous small-sig. model for MOS transistor in normal operation, IC simul. *Iniguez, B., +, T-CAD Feb 95 163-166*
- dc operating point anal., unstable operating points, IC design. *Green, M.M., +, T-CAD Mar 95 360-370*
- hysteretic I-V charact. modeling for reson. tunneling diodes. *Ming-Huei Shieh, +, T-CAD Sep 95 1098-1103*
- magnetotransistors, mag. field sensit. modelling, HSPICE. *Salim, A., +, T-CAD Apr 95 464-469*
- non-tree routing topologies for VLSI layout. *McCoy, B.A., +, T-CAD Jun 95 780-784*
- Nyquist data converters, verif., behavioral simul. *Liu, E., +, T-CAD Apr 95 493-502*
- quantum electronic devices, device and cct. simul. *Mohan, S., +, T-CAD Jun 95 653-662*
- RTD large-sig. DC model suitable for PSPICE. *Zhixin Yan, +, T-CAD Feb 95 167-172*

Stability; cf. Circuit stability; Numerical stability

Statistics

- combinat. ccts., fault coverage estim. by test vector sampling. *Heragu, K., +, T-CAD May 95 590-596*
- STYLE, stat. IC design based on perform. macromodeling. *Chen, J., +, T-CAD Jul 95 794-802*

Stochastic differential equations

- Si devices, thermal noise in math. models of quasi-homogen. reg. *Mamontov, Y.V., +, T-CAD Jul 95 815-823*

Surfaces; cf. Rough surfaces

Switched capacitor filters

- symbolic anal. of SC filtering networks, sig. flow graphs. *Fino, M.H., T-CAD Jul 95 858-867*

Switching circuits

- act. timing multilevel fault-simul., switch-level accuracy. *Meyer, W., T-CAD Oct 95 1241-1256*

Switching functions; cf. Logic functions

Switching transients

- CMOS mixed sig. ccts., substr. coupling models based on Voronoi tessellation. *Wemple, I.L., +, T-CAD Dec 95 1459-1469*

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Tessellation automata; cf. Cellular automata

Testing; cf. Automatic testing; Logic circuit testing

Thermal factors; cf. Semiconductor device thermal factors

Time delay; cf. Delay effects

Time difference of arrival estimation; cf. Delay estimation

Time domain analysis

- CFH, complex freq. hopping anal. of interconnect networks. *Chiprout, +, T-CAD Feb 95 186-200*
- MCM lossy coupled transm. line trees, time domain response, effic. approx. *Sriram, M., +, T-CAD Aug 95 1013-1024*
- nonlin. oscillatory ccts., steady-state output determ., multiple shoot. *Parkhurst, J.R., +, T-CAD Jul 95 882-889*

Time domain analysis; cf. FDTD methods

Time measurement; cf. Clocks

Time of arrival estimation; cf. Delay estimation

Timing

- act. timing multilevel fault-simul., switch-level accuracy. *Meyer, W., T-CAD Oct 95 1241-1256*
- combinat. logic cct. delay, functional timing anal., ATPG. *Ashar, P., T-CAD Aug 95 1025-1030*
- cyclic combinat. ccts., test generation. *Raghunathan, A., +, T-CAD Jul 95 1408-1414*
- delay-insensitive cct. behavior, realizability and synthesis. *Leung, S., +, T-CAD Jul 95 833-848*
- digital MOS macromodel accuracy improvement, series trans. reduction. *Jeong-Taek Kong, +, T-CAD Jul 95 868-881*
- GaAs DCFL ccts., timing macromodels. *Kayssi, A.I., +, T-CAD Mar 95 384-393*
- max.-rate single-phase closed pipeline clocking including v. pipelining/stoppability/startability. *Chang, C.-H., +, T-CAD Dec 95 1526-1545*
- pseudo-exhaustive built-in TPG for seq. ccts. *Kagaris, D., +, T-CAD Jul 95 1160-1171*
- std.-cell VLSI cct. design, timing/area optim. *Weitong Chuang, +, T-CAD Mar 95 308-320*
- symbolic anal. of SC filtering networks, sig. flow graphs. *Fino, M.H., T-CAD Jul 95 858-867*
- VLSI timing optim. by gate resizing and crit. path ident. *Chen-Liang Fu, +, T-CAD Feb 95 201-217*

Topology; cf. Circuit topology

Transducers; cf. Magnetic transducers

Transfer functions

- CFH, complex freq. hopping anal. of interconnect networks. *Chiprout, +, T-CAD Feb 95 186-200*
- lin. cct. anal. by Pade approx. via Lanczos proc. *Feldmann, P., +, T-CAD May 95 639-649*
- symbolic anal. of SC filtering networks, sig. flow graphs. *Fino, M.H., T-CAD Jul 95 858-867*

Transforms; cf. Laplace transforms

Transient analysis

- TRASIM, 2D transient simulator for planar semicond. devices. *Obrecht, M.S., +, T-CAD Apr 95 447-458*

Transient analysis; cf. Circuit transient analysis

Transistors; cf. Bipolar transistors; Magnetic transducers

Transmission lines; cf. Coupled transmission lines

Trees (graphs)

- MCM lossy coupled transm. line trees, time domain response, effic. approx. *Sriram, M., +, T-CAD Aug 95 1013-1024*
- near-optimal crit. sink routing tree constr. *Boese, K.D., +, T-CAD Dec 95 1417-1436*
- perform.-driven routing tree design, Prim-Dijkstra tradeoffs. *Alpert, C., +, T-CAD Jul 95 890-896*
- TRACER-fpga, router for RAM-based FPGAs. *Ching-Dong Chen, T-CAD Mar 95 371-374*

VLSI, optimal wiresizing under Elmore delay model. *Gong, J.J.*, +, *T-CAD Mar 95* 321-336

tunnel diodes
hysteretic I-V charact. modeling for reson. tunneling diodes. *Ming-Huei Shieh*, +, *T-CAD Sep 95* 1098-1103

U

ultra-large-scale integration
BPSG insulating film thermal flow, 3D modeling, surface diffusion. *Fujinaga, M.*, +, *T-CAD May 95* 631-638

uncertainty; cf. Fuzzy sets

user interfaces
TCAD syst., VISTA user interface and task level. *Halama, S.*, +, *T-CAD Oct 95* 1208-1222

V

very-large-scale integration
12th IEEE VLSI Test Symposium, selected papers (special issue). *T-CAD May 95* 529-612

3D MOSFET simul., massively parallel computation, splitting-up operator. *Odanaka, S.*, +, *T-CAD Jul 95* 824-832

bipolar ccts., robust simul. techs. based on waveform relax. *Wen Fang*, +, *T-CAD Apr 95* 510-518

BIST for VLSI ccts., test embedding, discrete logarithms. *Lempel, M.*, +, *T-CAD May 95* 554-566

channel pin assignment algs., perform. driven. *Her, T.W.*, +, *T-CAD Jul 95* 849-857

channel routing hierarchical pin permutation, preprocessor. *Chen, C.Y.R.*, +, *T-CAD Jul 95* 896-903

CMOS VLSI digital ccts., delay optim., transistor reordering. *Carlson, B.S.*, +, *T-CAD Oct 95* 1183-1192

CMOS VLSI digital ccts., power/ground buses, pattern independent max. current estim. *Kriplani, H.*, +, *T-CAD Aug 95* 998-1012

C-testable iter. logic arrays, BIST. *Gala, M.*, +, *T-CAD Nov 95* 1388-1398

datapath synthesis, problem-space genetic algm. *Dhodhi, M.K.*, +, *T-CAD Aug 95* 934-944

delay-insensitive cct. behavior, realizability and synthesis. *Leung, S.C.*, +, *T-CAD Jul 95* 833-848

digital MOS macromodel accuracy improvement, series transistor reduction. *Jeong-Taek Kong*, +, *T-CAD Jul 95* 868-881

floorplanning, area minimization problem. *Peichen Pan*, +, *T-CAD Jan 95* 123-132

hierarchical VLSI designs, squashing. *Kaser, O.*, *T-CAD Nov 95* 1398-1402

layout design, net assignment problem, routing constraint. *Ting-Chi Wang*, +, *T-CAD Feb 95* 265-269

levelized incomplete LU factorization, large-scale cct. simul. appl. *Eickhoff, K.-M.*, +, *T-CAD Jun 95* 720-727

multiway partitioning, geometric embeddings, orderings, dyn. prog. *Alpert, C.J.*, +, *T-CAD Nov 95* 1342-1358

near-optimal crit. sink routing tree constr. *Boese, K.D.*, +, *T-CAD Dec 95* 1417-1436

non-tree routing topologies for VLSI layout. *McCoy, B.A.*, +, *T-CAD Jun 95* 780-784

optimal wiresizing, Elmore delay model. *Gong, J.J.*, +, *T-CAD Mar 95* 321-336

over-the-cell channel routing and pin assignment. *Her, T.W.*, +, *T-CAD Jun 95* 766-772

perform.-driven routing tree design, Prim-Dijkstra tradeoffs. *Alpert, C.J.*, +, *T-CAD Jul 95* 890-896

pseudo-exhaustive testing, VLSI ccts., cct. partitioning and test generation method. *Wen-Ben Jone*, +, *T-CAD Mar 95* 374-384

RC parasitics modeling, network reduction algm. *Niewczas, M.*, +, *T-CAD Feb 95* 137-144

replication cut for two-way partitioning in VLSI cct. layout. *Lung-Tien Liu*, +, *T-CAD May 95* 623-630

segmented channel routing problem, complexity. *Wing Ning Li*, *T-CAD Apr 95* 518-523

single scan chain in VLSI designs, reconfig. techs. *Narayanan, S.*, +, *T-CAD Jun 95* 750-765

std. cells, pin permutation algm. for improving over-the-cell channel routing. *Chen, C.Y.R.*, +, *T-CAD Aug 95* 1030-1037

std.-cell VLSI cct. design, timing/area optim. *Weitong Chuang*, +, *T-CAD Mar 95* 308-320

symbolic trajectory eval. and BDDs, theorem prover, VLSI design. *Hazelhurst, S.*, +, *T-CAD Apr 95* 413-422

timing optim., gate resizing, crit. path ident. *Chen-Liang Fang*, +, *T-CAD Feb 95* 201-217

voltage depend. capacitance model, mfg. proc. variabilities, voltage coeffs. *Ito, A.*, *T-CAD Sep 95* 1093-1097

worst-case anal. and optim. of VLSI cct. performs. *Dharchoudhury, A.*, +, *T-CAD Apr 95* 481-492

VLSI Test Symposium, 12th (1994) IEEE
selected papers (special issue). *T-CAD May 95* 529-612

W

Wiring

cross point assignment, global rerouting for general-archit. designs. *Wen-Chung Kao*, +, *T-CAD Mar 95* 337-348

VLSI, optimal wiresizing under Elmore delay model. *Gong, J.J.*, +, *T-CAD Mar 95* 321-336

Y

Yield estimation

uneven fault coverage in ICs, quality reduction. *Maxwell, P.C.*, *T-CAD May 95* 603-607

Yield optimization

parametric yield optim., linearized perform. penalty method. *Krishna, K.*, +, *T-CAD Dec 95* 1557-1568

STYLE, stat. IC design based on perform. macromodeling. *Chen, J.*, +, *T-CAD Jul 95* 794-802

Z

Zeros; cf. Poles and zeros

FIRST ANNOUNCEMENT AND CALL FOR PAPERS

Sponsored by the ACM SIGDA, the IEEE Solid-State Circuits Council, and the IEEE Circuits and Systems Society

1996 INTERNATIONAL SYMPOSIUM ON LOW POWER ELECTRONICS AND DESIGN

Monterey Convention Center
Doubletree Hotel, Monterey, CA
August 12 - 14, 1996

The International Symposium on Low Power Electronics and Design provides a forum for the presentation of advances in low power systems and components. All aspects of designing a low power product, from fabrication technology and circuits to systems and software, are within the scope of the Symposium. Topics of interest include, but are not limited to:

Technology and Devices

- Technology and processing
- Batteries
- Displays
- Device design

Software and Systems

- Compilers & embedded systems
- Logic and module design
- Microprocessor design
- Power management and design

Digital Electronics

- Digital circuits
- Memories
- Micro-architecture
- Energy Recovery circuits

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- Behavioral & system level design aids
- Logic synthesis and physical design
- Digital circuit design
- Interconnect and package design

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- RF techniques
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Simulation and Estimation

- Algorithmic and architectural level
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- Power analysis and verification

This Symposium is the result of a merger between the Symposium on Low Power Electronics and the International Symposium on Low Power Design. Like its predecessors, the merged symposium will contain a mix of invited talks and contributed papers. However, the Symposium will consist of two parallel tracks: one focusing on systems and CAD, the other focusing on circuits and technology. All invited talks will be plenary and thus can be heard by all attendees. Contributed papers should report on significant advances in the field, and make clear what new ideas and results are being described. Reduction to hardware or practical application is desirable but not necessary.

SUBMISSION OF PAPERS

In general, submitted papers must describe original work which will not be announced or published elsewhere prior to the Symposium. However, overview/review papers of appropriate topics in low power electronics and design will also be considered. Submissions may range in length from abstracts of 500-750 words with supporting figures to full length papers of up to 5000 words. Submissions longer than 1000 words should include a 100-150 word abstract summarizing what is new and important in the paper. Submissions must include information on the contact person for the paper: name, full address (including street address for express delivery), telephone number, fax number, e-mail address. Authors must indicate in which of the six topic areas listed above the paper should be considered, and should submit 15 copies of the paper. DEADLINE FOR RECEIPT OF SUBMISSIONS IS MARCH 1, 1996. Authors of accepted papers will be notified by April 26. Accepted papers will be published in the Symposium Digest; final versions of the papers, up to 6 pages of camera-ready copy, will be due Friday, May 31, 1996. Authors of accepted papers must sign a copyright release form.

Proposals for panels are requested in all areas of low power design. Proposals must describe the topic, provide a list of participants with addresses and phone numbers, including moderator and contact. Proposals should be submitted to either of the Program Co-chairs by February 16, 1996.

All papers should be submitted to Massoud Pedram, Technical Program Co-Chair.

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